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PTO/SB/05 (1/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2987.2US (96-790.1)
First Inventor or Application Identifier	Michael B. Ball
Title	METHOD AND APPARATUS FOR ROUTING DIE INTERCONNECTIONS USING INTERMEDIATE CONNECTION ELEMENTS SECURED TO THE DIE FACE
Express Mail Label No.	EL500247802US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
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1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)

2. [X] Specification [Total Pages 18]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S C. 113)* [Total Sheets 11]

4. Oath or Declaration [Total Pages 1]
a. [ ] Newly executed (original or copy)
b. [X] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F R §§ 1 63(d)(2) and 1.33(b).

5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R §3 73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No 08 / 800,841

Prior application information: Examiner A. Chambliss Group / Art Unit: 2814

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

Name	Stephen R. Christian Trask, Britt & Rossa				
Address	P.O. Box 2550				
City	Salt Lake City	State	Utah	Zip Code	84110
Country	U.S.A.	Telephone	(801) 532-1922	Fax	(801) 531-9168

Name (Print/Type)	Stephen R. Christian	Registration No. (Attorney/Agent)	32,687
Signature		Date	03/16/2000

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PATENT
Attorney Docket 2987.2US (96-790.1)

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Express Mail Mailing Label Number: EL500247802US

Date of Deposit with USPS: March 16, 2000

Person making Deposit: Jared S Turner

APPLICATION FOR LETTERS PATENT

for

METHOD AND APPARATUS FOR ROUTING DIE INTERCONNECTIONS USING INTERMEDIATE CONNECTION ELEMENTS SECURED TO THE DIE FACE

Inventor:
Michael B. Ball

Attorneys:
Joseph A. Walkowski
Registration No. 28,765
Stephen R. Christian
Registration No 32,687
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

METHOD AND APPARATUS FOR ROUTING DIE INTERCONNECTIONS USING INTERMEDIATE CONNECTION ELEMENTS SECURED TO THE DIE FACE

BACKGROUND OF THE INVENTION

Cross Reference to Related Application: This application is a divisional of application Serial No. 08/800,841, filed February 14, 1997, pending.

Field of the Invention: This invention relates generally to a method and apparatus for routing die interconnections on a semiconductor die and, more specifically, to a method and apparatus for routing die interconnections using intermediate connection elements secured to a major surface of the die.

State of the Art: A typical integrated circuit (IC) or semiconductor die includes external connection points termed "bond pads" that are in electrical communication with integrated circuits formed in or on the active surface of the die. The bond pads are used to provide electrical connection between the integrated circuits and external devices, such as lead frames or printed circuit boards. The bond pads also provide sites for electrical testing of the die, typically by contact with probes, which send and receive signals to and from the die to evaluate the functionality of the die.

In a conventional die/lead frame assembly, the semiconductor die is attached to a die paddle of a lead frame using an adhesive or tape. The bond pads formed on the face of the die are typically electrically and mechanically attached to lead fingers terminating adjacent the periphery of the die using thin bonding wires of gold, aluminum or other metals or alloys. Other types of lead frames, such as so-called "leads over chip" (LOC) or "leads under chip" (LUC), dispense with the die paddle and support the die from portions of the lead fingers themselves.

Wire bonding is typically a process through which some or all of the bond pads formed on the face of the die are connected to the lead fingers or buses of a lead frame by thin bonding wires. The bonding wires comprise the electrical bridge between the bond pads and the leads of the packaged integrated circuit. A wire bonding apparatus bonds the bonding wires to the bond pads and to the lead fingers, typically using heat and

pressure, as well as ultrasonic vibration in some instances. Following wire bonding, the lead frame and die are typically encapsulated in a plastic (particle-filled polymer) or packaged in a preformed ceramic or metal package. After encapsulation, the lead fingers are then trimmed and usually bent to form external leads of a completed semiconductor package in what is termed a "trim and form" operation.

Another wire bonding application may include chip-on-board (COB), where the back-side surface of a bare IC die is directly mounted on the surface of a substantially rigid printed circuit board (PCB) or other carrier substrate, and bond pads on the front-side or active surface of the bare die are then wire bonded to wire bondable trace pads or terminals on the surface of the PCB to interconnect circuitry in the die with external circuitry through conductive traces on the PCB. Likewise, wire bondable traces may be formed from a metal film carried on a flexible polyimide or other dielectric film or sheet similar to those employed in so-called TAB (tape automated bonding) lead frame structures. A die may be back-mounted on the flex circuit and the traces wire bonded to bond pads on the surface of the die.

A typical die bond pad is formed as a rectangle or square typically having an area of less than 10^4 μm^2 and framed or bounded by a passivation layer on the face of the die. Bond pads are typically formed from a conductive metal such as aluminum and electrically connected to an underlying integrated circuit formed in or on the die. Usually a barrier layer and a polysilicon layer separate the bonding pad from an oxide layer of a silicon substrate in which the active semiconductor devices are formed. A passivation layer formed of a dielectric material (silicon dioxide, silicon nitride, polyimide, BPSG, etc.) or as a sandwich of different materials (e.g., silicon dioxide/silicon) covers the oxide layer, and the bond pad is embedded in the passivation layer. Such bond pads may be located generally along the peripheral edges of the die, inset from the edges a desired distance, or in one or more center rows. These bond pads are then typically wire bonded to a lead frame, thermocompression bonded to an overlying TAB tape or flip-chip bonded (with appropriate prior "bumping" of the bond pads) to a printed circuit board.

It is often desirable to interconnect various bond pads on a single semiconductor die in order to alter the input and/or output functionality of the die, such as when it is necessary to "wire around" defective portions of a die which is only partially functional. For example, a 16 megabit DRAM memory die may only demonstrate 11 megabits of functional memory under electrical testing and burn-in. Alternatively, it may be desirable for a die having a given input/output (bond pad) configuration to "look" to a particular lead frame or carrier substrate as if it were configured differently so that the die could be used with a lead frame for which it was not originally intended. Such "wire around" functions, where possible, are typically accomplished by interconnecting bond pads on the die through external circuitry in printed circuit boards or other carrier substrates to which the die is mounted. Where the desired input and/or output functionality configuration varies from die to die, a separately configured printed circuit board or other carrier substrate must be provided for each desired input and/or output functional configuration. Thus, it would be desirable to provide a relatively easy way of interconnecting selected bond pads on a single integrated circuit die without requiring the use of external circuitry in printed circuit boards and other carrier substrates.

SUMMARY OF THE INVENTION

Accordingly, a semiconductor die according to the present invention is comprised of a die bearing integrated circuits. Such integrated circuits may comprise a memory device, microprocessor, or any other semiconductor device or functional combination of devices. In a preferred embodiment, the active surface of the die (i.e., the surface of the die having bond pads thereon and bearing the integrated circuits) includes at least one electrically isolated intermediate connection element or wire-bondable jumper pad attached thereto, each bondable jumper pad being electrically isolated from external circuitry and from circuitry of the die, but for wire bonds extending to and/or from the bondable jumper pad. That is, each bondable jumper pad is not directly electrically connected to internal circuitry of the die, unlike the bond pads, but provides a "stepping stone" for wire bonds between bond pads of the die or between a bond pad and a

conductor external to the die. Thus, a relatively short wire bond can be formed from a bond pad to the jumper pad and another relatively short wire bond formed from the jumper pad to another bond pad (or external conductor) forming an electrical connection between the two bond pads (or bond pad and external conductor).

In another preferred embodiment, a plurality of jumper pads is provided over the active surface of the die, providing various serial jump points for a plurality of wire bonds to be formed in series between a plurality of bond pads. Where the semiconductor die has bond pads located about a peripheral edge of the active surface, a grid or array of jumper pads may be provided proximate the center of the active surface and at least partially bounded by the peripheral bond pads.

In yet another preferred embodiment, the semiconductor device is of the aforementioned LOC configuration and includes a lead frame having lead fingers and/or bus bars that extend over the active surface of the die. In addition, a plurality of jumper pads is provided on the active surface so that wire bonds can be made from bond pads to jumper pads to bus bar to jumper pad to bond pad to lead finger, or any combination thereof, depending on the desired input/output (I/O) configuration of the die.

Preferably, the jumper pads are comprised of a conductive material, such as metals (e.g., aluminum or gold) or alloys thereof.

In a preferred embodiment, the jumper pads are silk-screened onto the active surface of the die. The jumper pads may also be electrolessly plated, electroplated, or electrochemically deposited, printed, sprayed (through a mesh), adhesively attached or otherwise formed onto the active surface of the die.

In yet another preferred embodiment, the jumper pads are formed in a grid or array on one side of an adhesive tape or film. Such a tape or film could then be cut to size to fit the specific die. The tape could be attached to the die by thermosetting, application of pressure, or other methods, depending on the type of tape and adhesive employed.

In another preferred embodiment, the jumper pads may be formed over a segment of insulating or dielectric material, such as a non-conductive film or coating, that is

applied to the active surface of the die. The insulating material protects internal circuitry near the active surface from any interference or shorting that may be otherwise generated by the presence of the jumper pad or connections to the jumper pads.

In yet another preferred embodiment, a jumper pad adapter is attached to the active surface of the die by an adhesive. The adhesive may be a pressure sensitive adhesive, a thermosetting adhesive or any other suitable adhesives known in the art. The jumper pad adapter includes a plurality of conductive lines extending through the adapter from the lower surface thereof which provides electrical contact between the bond pads or conductive bumps formed on the die and contact pads formed on the top surface of the jumper pad adapter. Thus, jumper pads are formed on the upper surface of the adapter rather than on the active surface of the die, and the contact pads and jumper pads on the adapter lie in substantially the same plane. Accordingly, all wire bonds between jumper pads and contact pads can be formed in the same horizontal plane relative to the top surface of the jumper pad adapter.

Preferably, the jumper pad adapter includes access holes that extend through the adapter to allow access for wire bonds to be made to bond pads on the active surface of the die that would otherwise be covered by the adapter.

In another preferred embodiment of the jumper pad adapter, the adapter includes internal and/or external conductive paths which can route signals between jumper pads and to and between bond pads on the active surface of the die.

In yet another preferred embodiment, an adapter, which converts a die having peripherally mounted bond pads to a flip-chip array connection configuration, includes first contact pads electrically connected to the bond pads of the die, second contact pads exposed on the top of the adapter and in horizontally-offset locations from the bond pads, and conductors extending to and between the first and second contact pads. The second contact pads may be bumped so that the adapter, and thus the die, can be flip-chip bonded to a PCB or other carrier substrate.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIGS. 1A and 1B are top and side views, respectively, of a first embodiment of a semiconductor device in accordance with the present invention;

FIG. 1C is a cross-sectional side view of a second embodiment of a semiconductor device illustrated in FIG. 1A;

FIGS. 2A and 2B are top and side views, respectively, of a third embodiment of a semiconductor device in accordance with the present invention;

FIG. 3 is an exploded cross-sectional side view of a fourth embodiment of a semiconductor device in accordance with the present invention;

FIG. 3A is a cross-sectional side view of the semiconductor device shown in FIG. 3 after assembly and application of a protective coating;

FIG. 4 is a top view of a fifth embodiment of a semiconductor device wire bonded to a lead frame in accordance with the present invention;

FIG. 5A is a top view of a sixth embodiment of a semiconductor device wire bonded to a lead frame in accordance with the present invention;

FIG. 5B is a cross-sectional side view of the embodiment illustrated in FIG. 5A;

FIG. 6 is a cross-sectional side view of a seventh embodiment of a semiconductor device in accordance with the present invention;

FIG. 6A is a cross-sectional side view of an eighth embodiment of a semiconductor device in accordance with the present invention;

FIG. 6B is a cross-sectional side view of an ninth embodiment of a semiconductor device in accordance with the present invention;

FIG. 7 is a top view of a semiconductor wafer comprising a plurality of the semiconductor device illustrated in FIG. 1A; and

FIG. 8 is a block diagram of an electronic system incorporating the semiconductor device of FIG. 1A.

DETAILED DESCRIPTION OF THE INVENTION

As illustrated in FIGS. 1A and 1B, a preferred embodiment of a semiconductor device 10 of the present invention includes a die 12 of generally rectangular configuration. The die 12 has an active surface 14 carrying a plurality of bond pads 16 proximate its perimeter 18 and a plurality of jumper pads 20, distinguished by surface shading in the drawing and disposed between the rows of peripheral bond pads 16. The bond pads 16 are formed as an integral part of the die 12, making contact with and providing an external contact for internal circuitry (not shown) contained within the die 12, as is known in the art.

As indicated, the bond pads 16 are typically formed in the active surface 14 of the die 12 and thus extend a distance into the active surface 14 through a passivation layer 21 (illustrated in FIG. 1C) to make electrical contact with the internal circuitry of the die 12. The jumper pads 20, on the other hand, are formed on the active surface 14 but are electrically isolated from the internal circuitry of the die 12. Moreover, the jumper pads 20 are preferably formed from a conductive material such as a metal, metal alloy, or any other suitable material known in the art to which a wire bond can be attached. The jumper pads 20 may be silk-screened, printed, sprayed through a patterned mesh, electrochemically deposited, or electroplated, electrolessly plated or otherwise attached to the active surface. Similarly, as shown in FIG. 1C, the jumper pads 20 may be preformed, and each adhesively attached to the active surface 14 with an adhesive 22, such as an epoxy or other similar material known in the art. The adhesive 22 is preferably insulative, although it does not have to be if the passivation layer 21 possesses sufficiently robust dielectric characteristics.

In FIGS. 2A and 2B, a semiconductor device 30 having peripheral bond pads 116 includes a sheet-like insulating layer, film or tape segment 32 disposed between an active surface 114 and jumper pads 120. The jumper pads 120 are thus formed in or on the tape 32 and the tape 32 is adhesively attached to the active surface 14 of a die 34. The tape 32 may be an adhesive-type tape or bear a thermosetting adhesive 33, one preferred tape being a polyimide film as sold under the trademark Kapton®, or other suitable tapes,

tape-like films or sheet structures adhesively attached to active surface 114 using adhesive techniques known in the art. Preferably, the tape 32 is non-conductive, and thus insulates the active surface 114 of the die 34 from electrical signals that may be passed through the jumper pads 120. The thickness of tape 32 has been exaggerated for clarity but may, in fact, be extremely thin, only of sufficient structural integrity to maintain its form during handling and application to the die.

FIG. 3 illustrates yet another preferred embodiment of a semiconductor device 40 according to the present invention in which an adapter 46 converts a peripherally bond padded semiconductor die 42 to a device 40 bearing jumper pads 220. The semiconductor die 42 includes bond pads 216 which have been "bumped;" that is, balls or bumps 44 of gold, solder or conductive adhesive have been attached thereto. An adapter 46 configured to mate with the active surface 214 and bond pads 216 of the die 42 is comprised of a support structure 48, which may be formed of a sheet-like structure, such as Kapton® or other tape as used in tape automated bonding, or a more rigid structure formed from ceramic, silicon, FR-4 or other materials known in the art. Preferably, the adapter 46 is formed from a material having a coefficient of thermal expansion (CTE) substantially matching the CTE of the die 42. The adapter 46 includes a plurality of first contact pads 50 on a top surface 52 and a plurality of second contact pads 54 proximate a bottom surface 56. The first contact pads 50 are electrically connected to the second contact pads 52 by conductive contacts or vias 58 that extend to and between the first and second contact pads 50 and 52, respectively, and are contained within the support structure 48. The second contact pads 54 are arranged to match the arrangement of bumped bond pads 216. Thus, when the adapter 46 and die 42 are brought together and mutually secured by adhesive 57, the second contact pads 54 mate with the bumped pads 216. As further illustrated in FIG. 3A, the assembled semiconductor device 40 may be dipped or coated with a protective layer 59 of, for example, epoxy or silicon gel to protect and insulate the adapter 46 and the die 42, and the contact pads 50 may be bumped so that the conductive bumps 61 extend above the protective layer 59 for flip-chip connection to a carrier substrate. In such an arrangement,

short conductive traces formed on the carrier substrate would extend between jumper pads 220 and contact pads 50 to be connected, a series of jumper pads 220, a contact pad 50 and an external circuit trace, etc. Alternatively, and as more fully described with respect to FIG. 6, rerouting circuitry may be carried within adapter 46 to reroute a bond pad 216 to a new location of a contact pad 50. It is also an option to employ adapter 46 only as an interposer substrate to provide for flip-chip connection of die 42 to a carrier substrate, omitting jumper pads 220 or any sort of bond pad rerouting capability.

As shown in FIG. 4, a semiconductor device 60, such as those illustrated in FIGS. 1A, 1B, 1C, 2A, 2B and 3, can be mounted to a conventional lead frame 62 as is known in the art. The lead frame 62 includes a plurality of lead fingers 66 extending outwardly from proximate the perimeter 67 of a die 70 and a die paddle 68 which supports the die 70 relative to the lead fingers 66. The lead fingers 66 form leads for a packaged semiconductor device (the outline of which is indicated by dashed line 72) after transfer-molded polymer encapsulation of the die 70 and lead frame 62 as is known in the art.

Conventionally, any connections to be made between bond pads 316, other than those made with circuitry internal to the die 70, are made through external circuitry, such as that contained in a printed circuit board to which the semiconductor device 60 is connected. This approach, however, requires a permanently configured product, namely the printed circuit board or other carrier substrate. The semiconductor device 60 of the present invention provides for flexibility in input/output (I/O) configurations of the device 60 that can be changed from device to device in the manufacturing process.

As illustrated, wire bonds 80, 81, 82, 83 and 84 can be formed: between bond pad 316 and lead finger 66; between adjacent or proximate bond pads 316; between, adjacent or proximate jumper pads 320; between bond pad 316 and jumper pad 320; or between jumper pad 320 and lead finger 66. The termination points of wire bonds 80, 81, 82, 83 and 84 can be of ball, wedge, or other configuration as is known in the art, and formed with a conventional wire bonding machine. Accordingly, a large number of I/O

alternative configurations can be achieved for any semiconductor device, depending on the number and layout of jumper pads 320 and configuration of wire bonds.

It is contemplated that any semiconductor die having bond pads thereon can benefit from the jumper pads in accordance with the present invention. In addition, such a die can be combined with any lead frame known in the art, such as a leads-over-chip (LOC) lead frame, or a hybrid frame, such as a lead frame 90 illustrated in FIG. 5A, that includes lead fingers or bus bars 92, 93, 94, and 95 extending over the active surface 414 of a die 96. Wire bonds 98 can thus be made between jumper pads 420 and lead fingers or bus bars 92, 93, 94 and 95 as well as those combinations described with reference to FIG. 4.

As illustrated in FIGS. 5A and 5B, a tape-like structure 100 adhesively attached to the active surface 414 and which supports the jumper pads 420 above the active surface 414 of the die 96 is provided with through holes or windows 102 to expose bond pads 416 located on the active surface 414 that would otherwise be covered by the sheet, film or tape-like structure 100. A wire bond 104 can thus be made between an exposed bond pad 416 and bus bar 93. Preferably, the bus bars 92, 93, 94, and 95 are attached with an adhesive 105 to the top surface 106 of the tape-like structure 100, with the sheet, film or tape-like structure likewise being adhesively attached as at 101 to the active surface 414 of the die 96. Thus, the bus bars 92, 93, 94, and 95 effectively support the die 96 relative to the rest of the lead frame 90.

In another preferred embodiment of the present invention shown in FIG. 6, a tape-like structure 110 may include its own internal circuitry or conductive lines 112 that connect jumper pads 520 to other jumper pads 520 and/or jumper pads 520 to bond pads 516 which are located on an active surface 514 of a die 512, and which are covered by the tape-like structure 110. It is also contemplated, as further illustrated, that the present invention has equal utility for multiple dice 512 and 513 in the same package (such as in a multi-chip module, or MCM) where wire bonds 515 make die-to-die interconnections between jumper pads 521 and/or bond pad 516 between the dice 512

and 513, as well as those combinations described with reference to single die 70 of FIG. 4.

It is contemplated that jumper pads in accordance with the present invention may also be advantageous to any situation where wire bonds are formed between a semiconductor die and external circuitry. For example, as illustrated in FIG. 6A, jumper pads 530 may be employed on a die 532 that is wire bonded to the leads 534 of a flex circuit 536. Likewise, as shown in FIG. 6B, jumper pads 540 may be formed on a die 542 that is directly mounted on a rigid PCB or carrier substrate 544 in a COB configuration with wire bonds 546 that are formed between jumper pads 540 and bond pads 548 and traces 550 on the PCB 544.

Those skilled in the art will appreciate that semiconductor devices according to the present invention may comprise an integrated circuit die employed for storing or processing digital information, including, for example, a Dynamic Random Access Memory (DRAM) integrated circuit die, a Static Random Access Memory (SRAM) integrated circuit die, a Synchronous Graphics Random Access Memory (SGRAM) integrated circuit die, a Programmable Read-Only Memory (PROM) integrated circuit die, an Electrically Erasable PROM (EEPROM) integrated circuit die, a flash memory die and a microprocessor die, and that the present invention includes such devices within its scope. In addition, it will be understood that the shape, size, and configuration of bond pads, jumper pads, dice, and lead frames may be varied without departing from the scope of the invention and appended claims. For example, the jumper pads may be round, oblong, hemispherical or variously shaped and sized so long as the jumper pads provide enough surface area to accept attachment of one or more wire bonds thereto. In addition, the bond pads may be positioned at any location on the active surface of the die.

As shown in FIG. 7, a semiconductor wafer 620 incorporates a plurality of integrated circuit dice 12 (shown in increased scale and reduced numbers relative to the wafer 620) of FIGS. 1A and 1B. Also, as shown in FIG. 8, an electronic system 130 includes an input device 132 and an output device 134 coupled to a processor device 136 which, in turn, is coupled to a memory device 138 incorporating the exemplary integrated circuit die 12 of FIGS. 1A and 1B.

Accordingly, the claims appended hereto are written to encompass all semiconductor devices including those mentioned. Those skilled in the art will also appreciate that various combinations and obvious modifications of the preferred embodiments may be made without departing from the spirit of this invention and the scope of the accompanying claims.

CLAIMS

What is claimed is:

1. An apparatus for routing interconnections among bond pads on a semiconductor die, comprising:

a sheet-like, non-conductive structure having a first surface, and a second surface for attachment to a die; and

a plurality of electrically conductive discrete pads attached to said first surface, the plurality of electrically conductive discrete pads electrically isolated from the second surface.

2. The apparatus of claim 1, further comprising at least one conductor extending between at least two of said plurality of electrically conductive discrete pads.

3. The apparatus of claim 1, further comprising at least one conductor extending from at least one bond pad of said die to at least one of said plurality of electrically conductive discrete pads.

4. The apparatus of claim 1, wherein said non-conductive structure is comprised of a dielectric film or sheet.

5 A method of routing external interconnections among a plurality of bond pads on an active surface of at least one semiconductor die, comprising:

providing at least one electrically conductive discrete pad on said active surface of said at least one semiconductor die in electrical isolation from said active surface; and

wire bonding from one of said plurality of bond pads to said at least one electrically conductive discrete pad.

6. The method of claim 5, further comprising wire bonding from said at least one electrically conductive discrete pad to another of said plurality of bond pads.

7. The method of claim 5, further comprising wire bonding from said at least one electrically conductive discrete pad to another electrically conductive discrete pad.

8. The method of claim 5, wherein providing said at least one electrically conductive discrete pad is provided by performing at least one of the group comprising silk screening, printing, spraying, electrochemically depositing, masking and etching, electroplating, electrolessly plating, and adhesively attaching.

9. The method of claim 5, further comprising:
attaching said at least one electrically conductive discrete pad to an insulating material; and attaching said insulating material to said die active surface.

10. The method of claim 9, further comprising selecting said insulating material from the group comprising thermosetting tape and adhesive tape.

11. The method of claim 5, further comprising selecting a material comprising said at least one electrically conductive discrete pad from the group comprising metals, alloys, and conductive epoxies.

12. The method of claim 5, further comprising:
providing a lead frame; and
attaching said at least one semiconductor die to said lead frame, said lead frame including:
a plurality of lead fingers proximate said at least one semiconductor die.

13. The method of claim 12, further comprising wire bonding from said at least one electrically conductive discrete pad to one of said plurality of lead fingers.

14. The method of claim 12, further comprising:

providing said lead frame with at least one bus bar, said bus bar extending over at least a portion of said active surface of said at least one semiconductor die; and

wire bonding from said at least one electrically conductive discrete pad to said at least one bus bar.

15. A semiconductor device, comprising:

a die including a plurality of bond pads disposed on a surface thereof;

an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads and said adapter having a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts in electrical communication with said first plurality of discrete electrical contacts; and

a plurality of conductive bumps, each extending from one of said second plurality of discrete electrical contacts.

16. The semiconductor device of claim 15, further comprising a protective coating over at least a portion of said die and with said plurality of conductive bumps being at least partially exposed.

17. A semiconductor device, comprising:

a die including a plurality of bond pads disposed on a first surface thereof;

an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts being horizontally remote from at least some of the bond pads disposed on the first surface of the die, the at least some of said second plurality of discrete electrical contacts being electrically

connected to said first plurality of discrete electrical contacts horizontally offset therefrom through conductors carried by said adapter.

18. The semiconductor device of claim 15, wherein the adapter comprises a material having a coefficient of thermal expansion substantially matching a coefficient of thermal expansion of said die.

19. The semiconductor device of claim 15, wherein the adapter comprises at least one conductive via extending between at least one of the first plurality of discrete electrical contacts and at least one of the second plurality of discrete electrical contacts.

20. The semiconductor device of claim 19, wherein at least some of the second plurality of discrete electrical contacts are electrically isolated from the bond pads disposed on the surface of the die.

21. The semiconductor device of claim 15, wherein the adapter is adhesively secured to the die.

22. The semiconductor device of claim 17, wherein the adapter is adhesively secured to the die.

23. The semiconductor device of claim 17, wherein at least one of the conductors carried by the adapter are internal to the adaptor.

24. The semiconductor device of claim 17, wherein the adapter comprises a tape-like structure.

25. The semiconductor device of claim 17, wherein at least one of the second plurality of discrete electrical contacts is electrically interconnected with a second die.

ABSTRACT OF THE DISCLOSURE

A semiconductor device, such as an integrated circuit die, includes a plurality of bond pads on an active surface thereof electrically connected to internal circuitry of the semiconductor device, and a plurality of jumper pads on the active surface which are electrically isolated from internal circuitry of the die. The jumper pads effectively provide stepping stones for wire bonds to be made across the active surface between bond pads. The jumper pads may be formed directly on the semiconductor device or on a non-conductive support structure that is attached to the semiconductor device.

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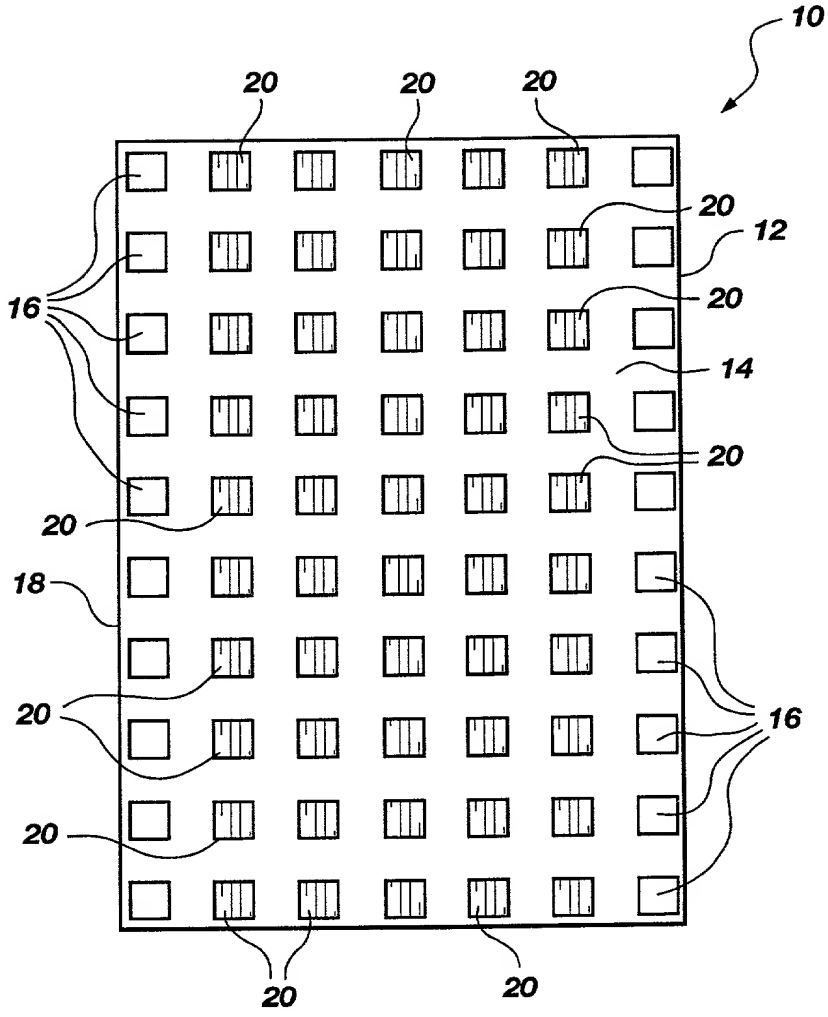

Fig. 1A

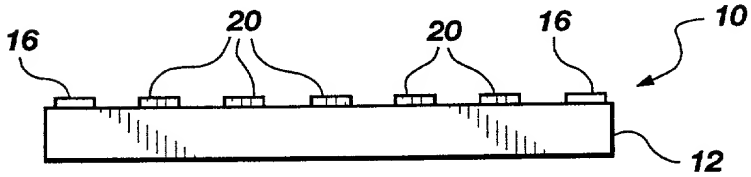

Fig. 1B

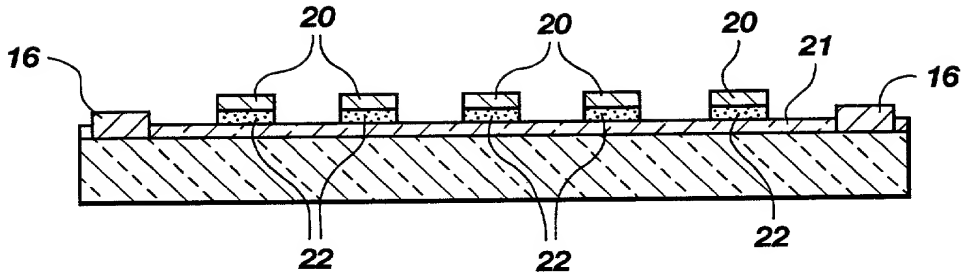

Fig. 1C

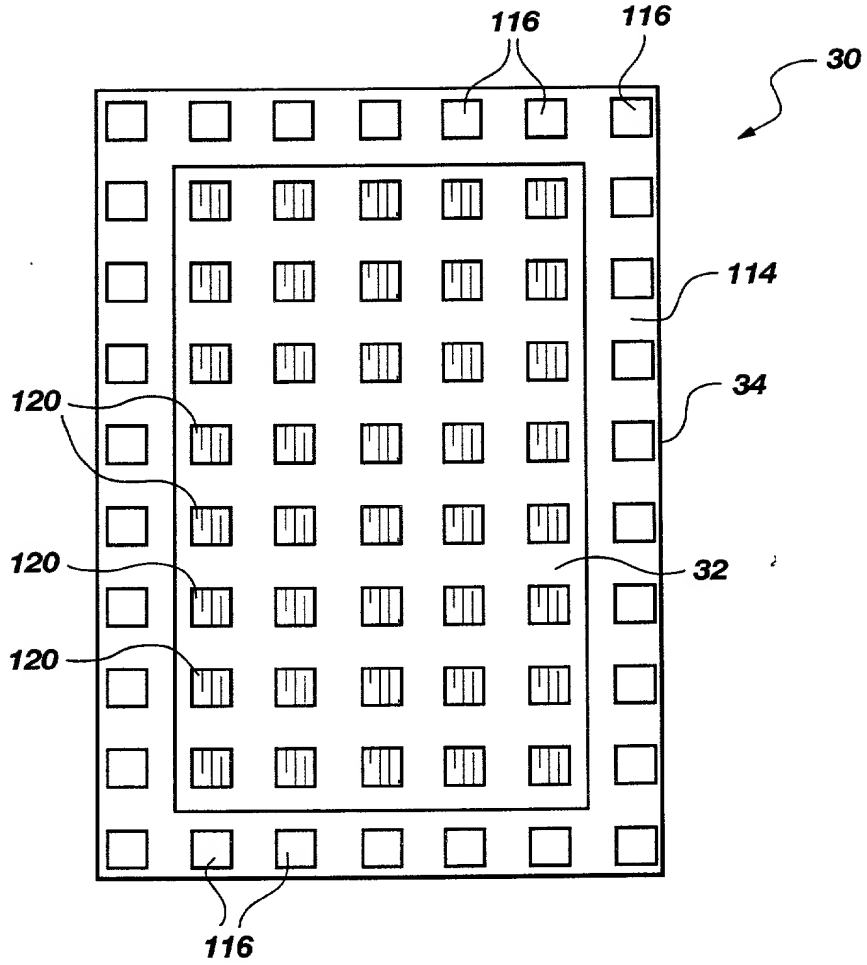
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Fig. 2A

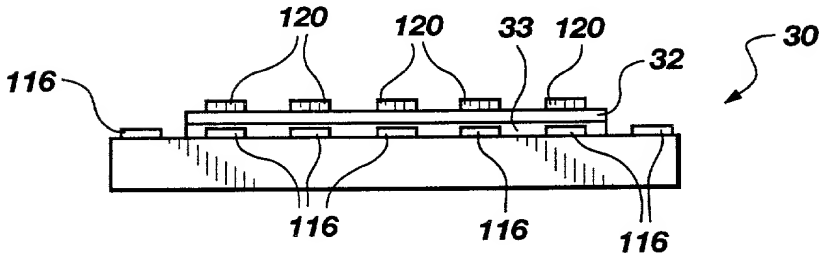
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Fig. 2B

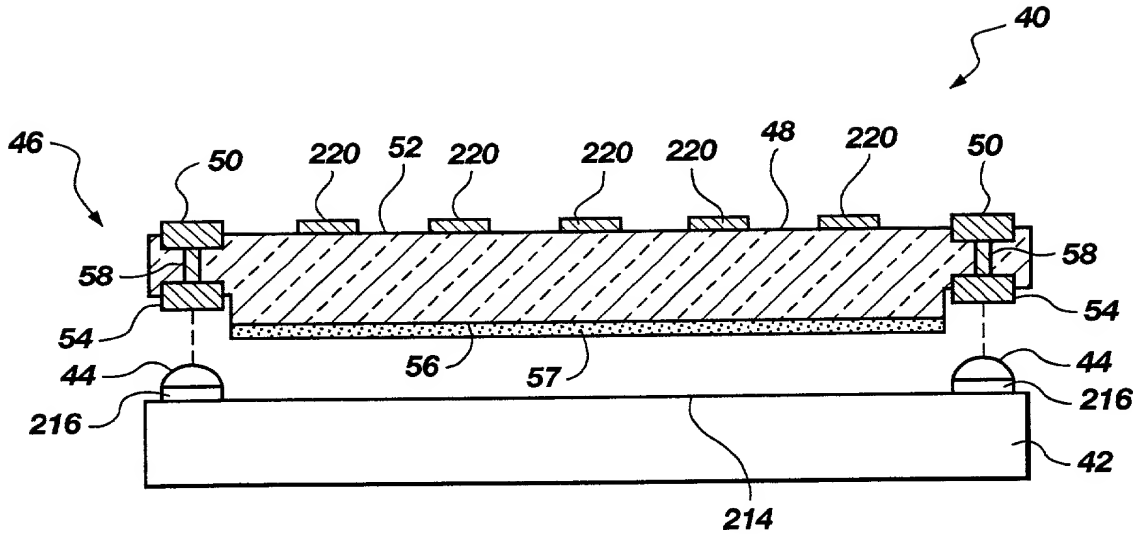
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Fig. 3

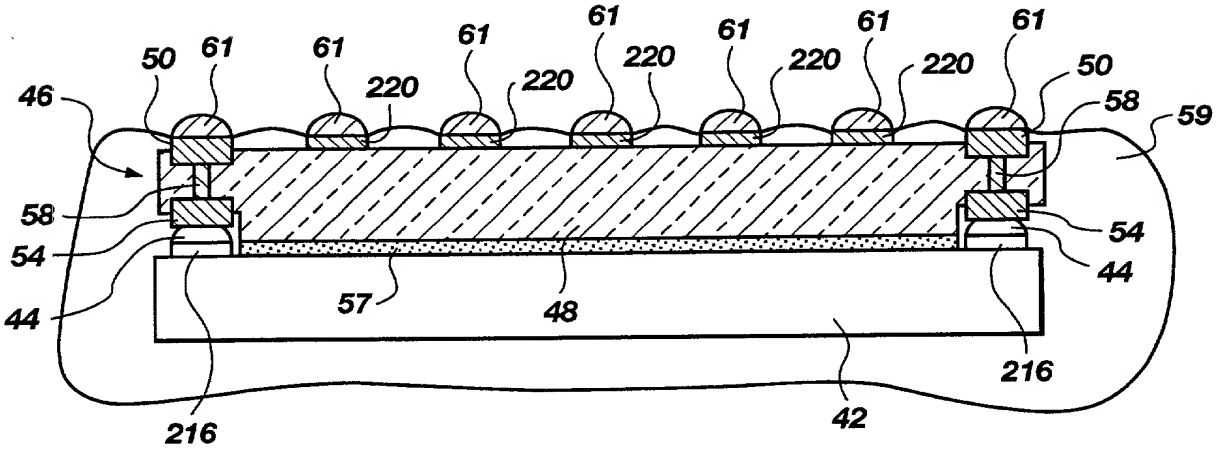
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Fig. 3A

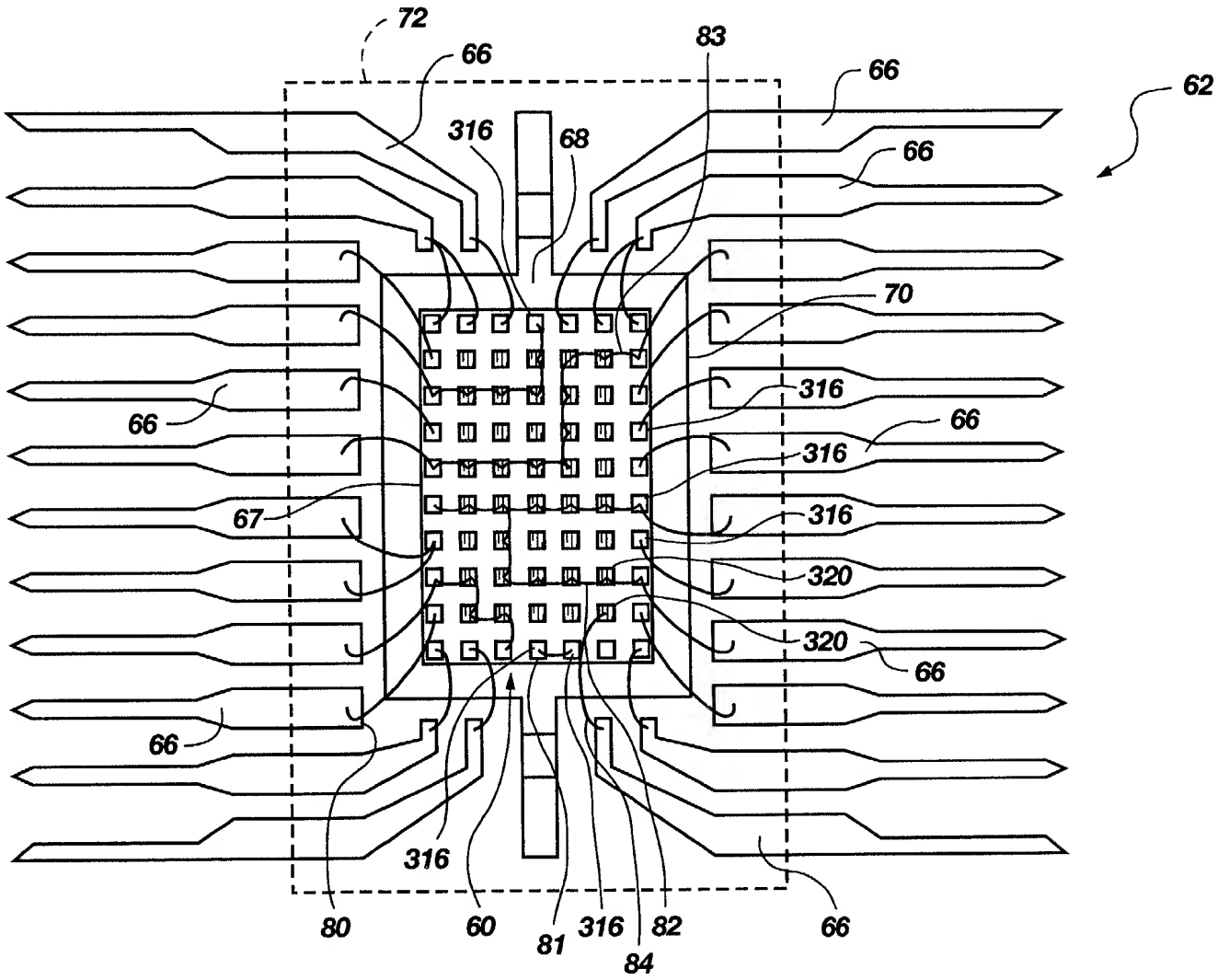

Fig. 4

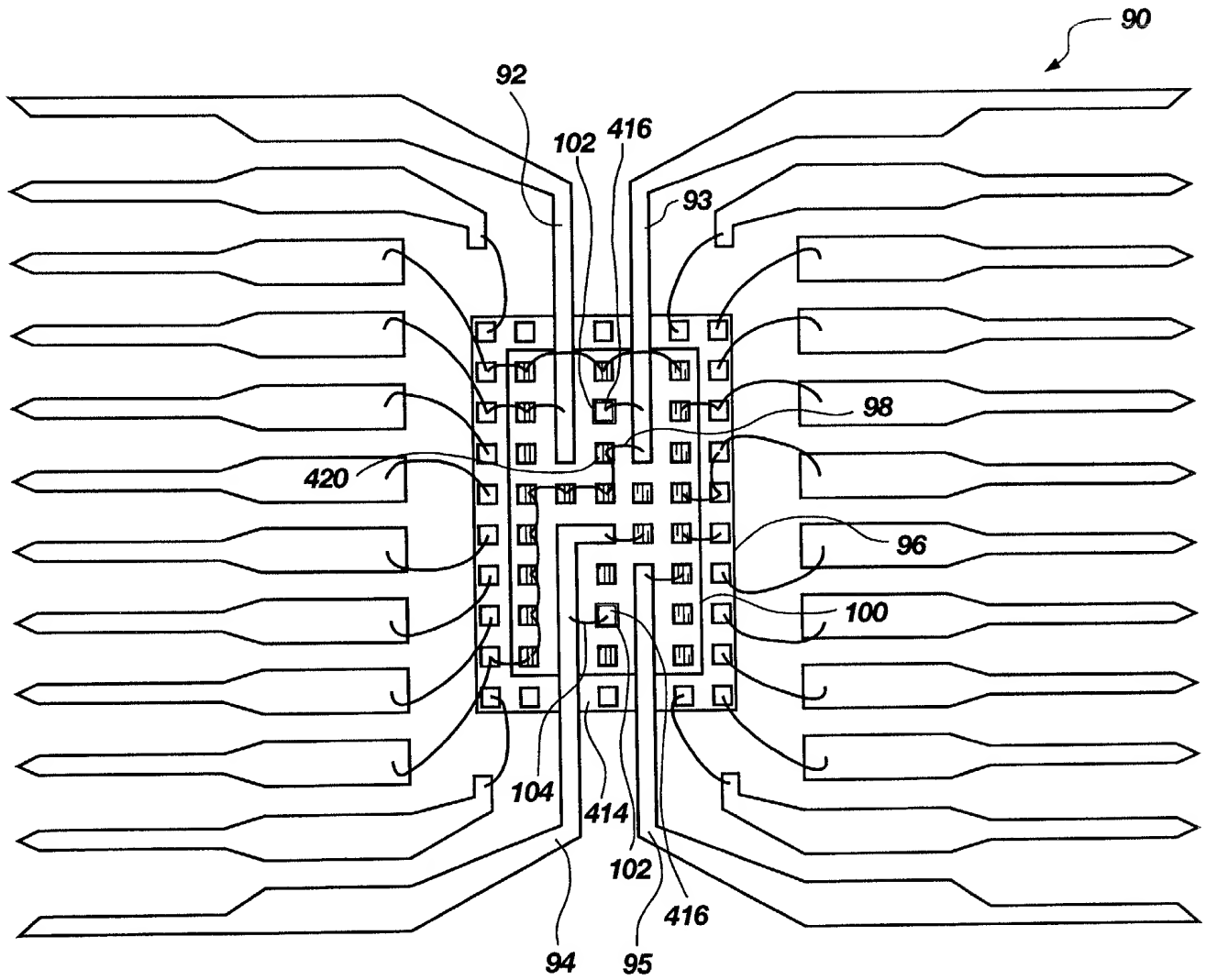

Fig. 5A

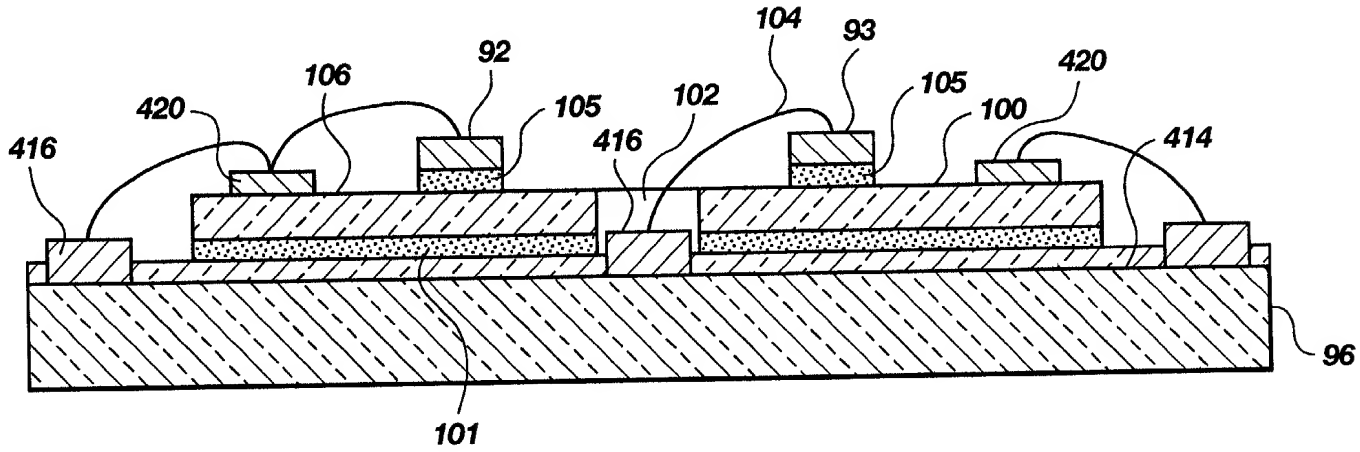

Fig. 5B

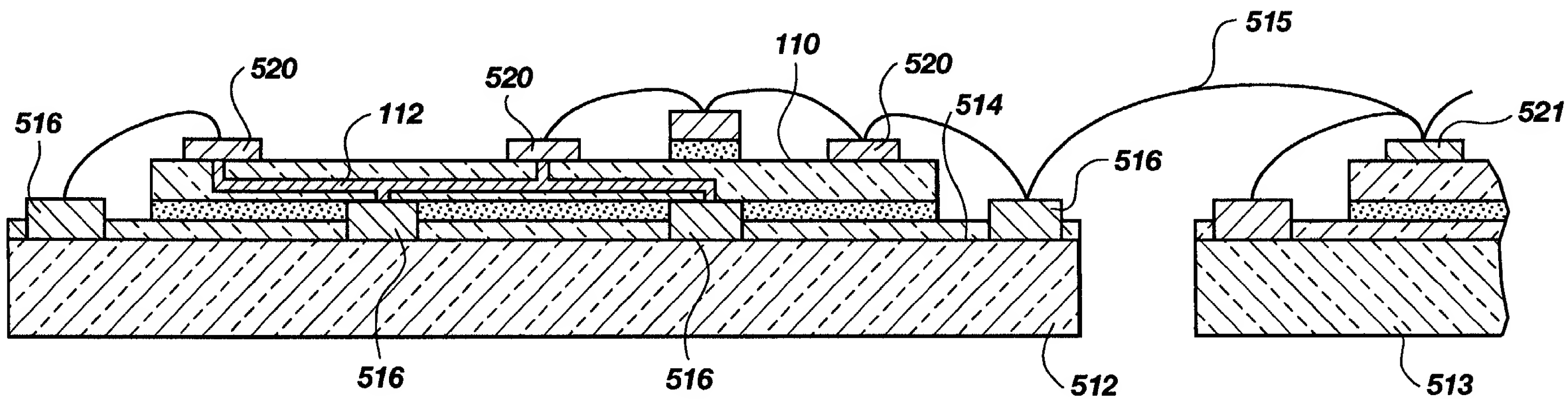

Fig. 6

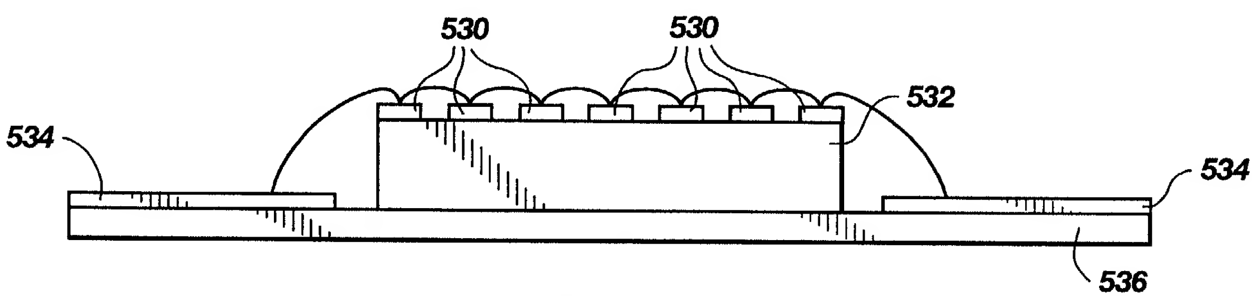
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Fig. 6A

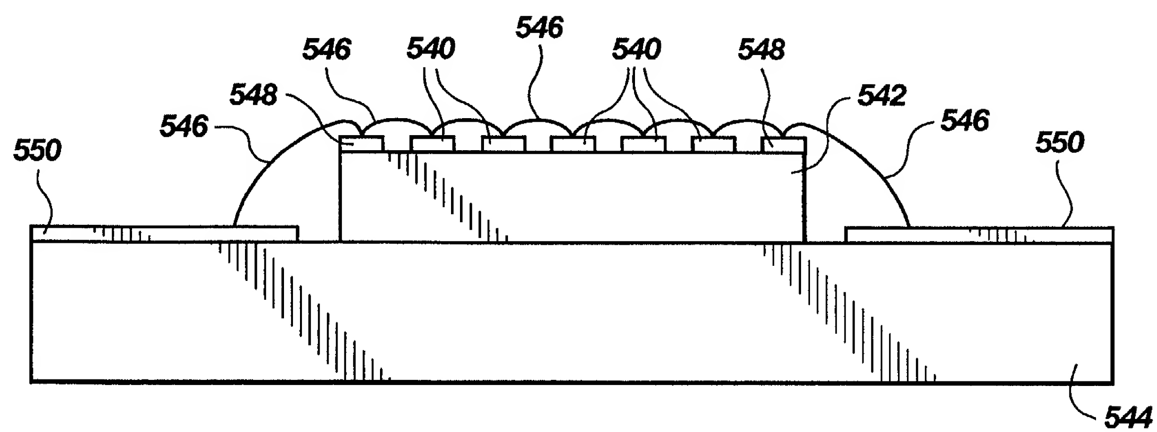
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Fig. 6B

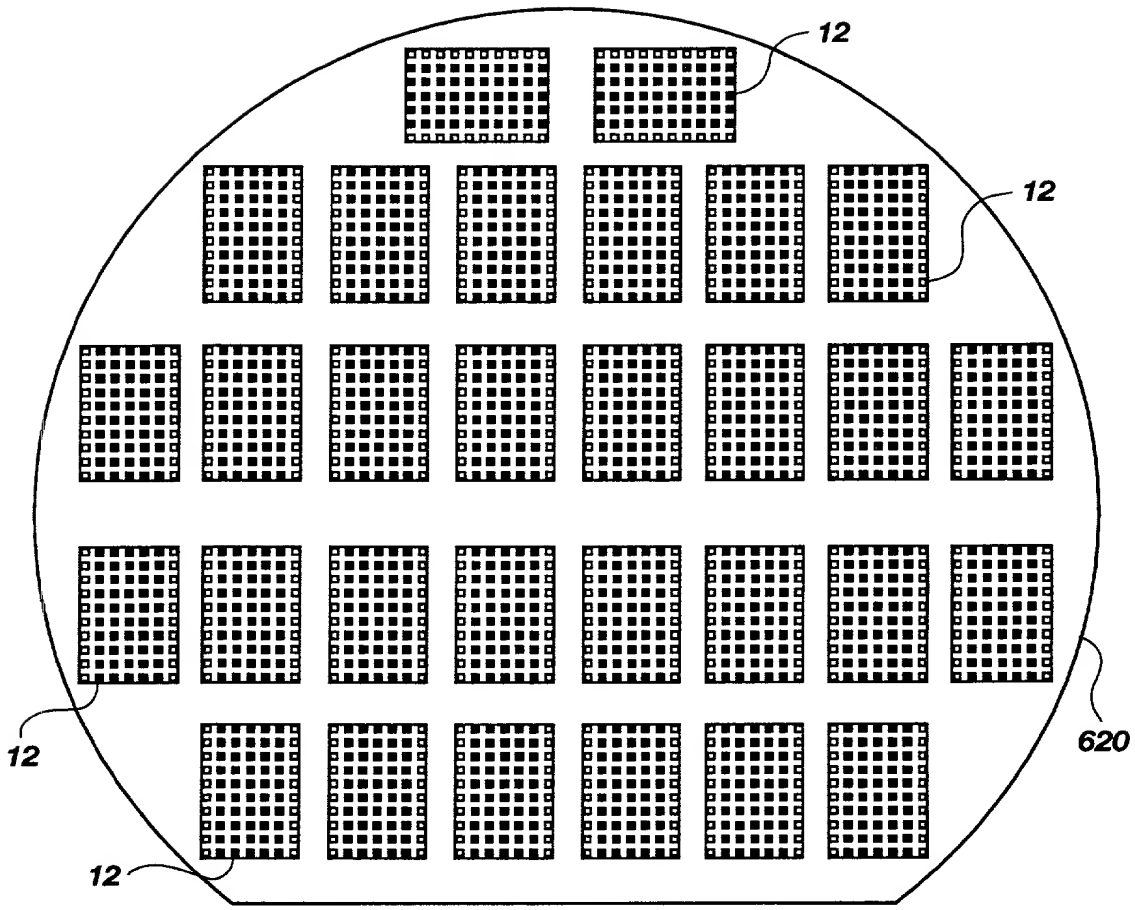
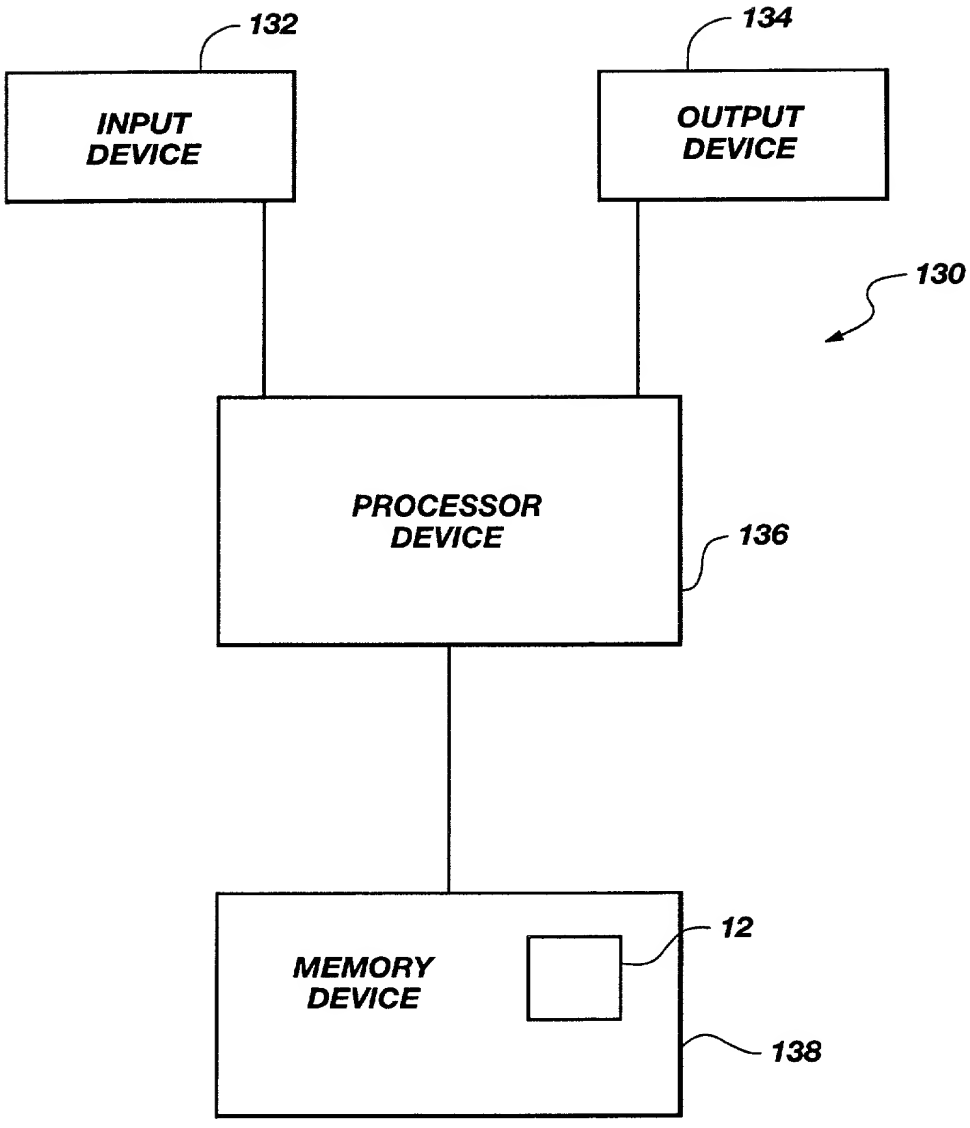


Fig. 7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INPUT DEVICE
OUTPUT DEVICE
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PROCESSOR DEVICE
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MEMORY DEVICE
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Fig. 8

Attorney Docket No. 2987US

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND APPARATUS FOR ROUTING DIE INTERCONNECTIONS USING INTERMEDIATE CONNECTION ELEMENTS SECURED TO THE DIE FACE, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
(provisional application no.)	(filing date)
(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Julie K. Morriss, Reg. No. 33,263
Robert G. Winkle, Reg. No. 37,474	Patrick McBride, Reg. No. 39,295	Edgar R. Cataxinos, Reg. No. 39,931
Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095	

Address all correspondence to: Joseph A. Walkowski, telephone no. (801) 532-1922.
TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Michael B. Ball
Inventor's signature Michael B Ball Date 2/3/97
Residence: Boise, Idaho 83704
Citizenship: U.S.A.
Post Office Address: 8630 Pembrook Drive, Boise, Idaho 83704